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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/802,735	03/18/2004	Yutaka Takafuji	1035-501	5007

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EXAMINER

TRAN, THIEN F

ART UNIT

PAPER NUMBER

2811

DATE MAILED: 12/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/802,735

Applicant(s)

TAKAFUJI ET AL.

Examiner

Thien F Tran

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 12 October 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-42 is/are pending in the application.
- 4a) Of the above claim(s) 6-8, 11 and 17-42 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5, 9, 10 and 12-16 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 06/25/04.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

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## **DETAILED ACTION**

### ***Election/Restrictions***

Applicant's election without traverse of species 1, claims 1-5, 9, 10, and 12-16, in the reply filed on 10/12/2004 is acknowledged.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 9 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 9 recites the limitation "the transistor" in line 2. There is insufficient antecedent basis for this limitation in the claim.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Yasukawa (USPN 6,232,142).

Yasukawa discloses the claimed semiconductor device (Figure 3e) comprising an insulating substrate 1 having a surface on which an SiO<sub>2</sub> film 3 is formed; and a remaining part (2, 5) of the single crystal silicon substrate (20, 5) being on the insulating

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substrate 1, wherein the single crystal silicon substrate (20, 5) includes a single crystal silicon thin film 2 and on which an SiO<sub>2</sub> film 5 formed, the surface of the insulating substrate 1, where the SiO<sub>2</sub> film 3 is formed, is bonded with the surface of the single crystal silicon substrate, where the SiO<sub>2</sub> film 5 is formed.

The claim limitations “a BOX layer, a hydrogen ion implantation section in which distribution of hydrogens peaks in the BOX layer” and “a part of the single crystal silicon substrate is separated at the hydrogen ion implantation section, and the BOX layer is removed from a remaining part of the single crystal silicon substrate” in claim 1 are taken to be product by process limitations. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al., 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product “gleaned” from the process steps, which must be determined in a “product by process” claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in “product by process” claims or not.

Regarding claim 3, the single crystal silicon thin film 2 is about 0.05 um which is about 50 nm thick (column 13, lines 46-49).

Regarding claim 16, the single crystal silicon thin film is formed on a substantially entire surface of the insulating substrate.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasukawa (USPN 6,232,142) in view of Yudasaka (JP 06-11729).

Yasukawa as described above does not disclose a non single crystal silicon thin film formed in a different region on the insulating substrate. Yudasaka discloses a semiconductor device comprising a single crystal silicon thin film 202 and a non single crystal silicon thin film (polysilicon 204) formed in different regions on the insulating substrate 201. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to form a single crystal silicon thin film and a non single crystal silicon thin film formed in different regions on the insulating substrate 1 as taught by Yudasaka in order to provide two different types of transistors on the same insulating substrate so that the operation speed of the peripheral circuit to drive an active matrix can be increased.

Claims 4 and 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasukawa (USPN 6,232,142).

Yasukawa as described above does not specifically disclose the single crystal silicon thin film 2 being about not more than 20 nm thick. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the thickness of the single crystal silicon thin film having the claimed range of thickness to

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reduce the device size as small as possible, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claims 12-13, Yasukawa does not specifically disclose the insulating substrate 1 being made of any one of a barium borosilicate glass, a barium alumino borosilicate glass, an alkaline earth alumino borosilicate glass, a borosilicate glass, an alkaline earth-zinc-lead-alumino borosilicate glass, and an alkaline earth-lead-alumino borosilicate glass. However, a barium borosilicate glass, a barium alumino borosilicate glass, an alkaline earth alumino borosilicate glass, a borosilicate glass, an alkaline earth-zinc-lead-alumino borosilicate glass, and an alkaline earth-lead-alumino borosilicate glass are insulating materials known in the art that are routinely used for the insulating substrate. Therefore, it would have been obvious modification to use either one of these known materials as a suitable material for the insulating substrate 1.

Regarding claim 14, Yasukawa discloses the same structure as claimed wherein the insulating substrate 1 and the single crystal silicon substrate 2 have the same materials as those used in the instant invention. Therefore, it is inherent that the structure of Yasukawa provides the same characteristics as claimed wherein a difference of linear expansion between the insulating substrate and the single crystal silicon substrate is about not more than 250 ppm at temperatures in a range between substantially room temperatures and 600°C.

Regarding claim 15, the insulating substrate 1 has the same materials as the material used for the insulating substrate in the instant invention. These materials for

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the insulating substrate 1 are inherently high-strain-point glasses whose strain point is not less than 500°C.


***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thien F Tran whose telephone number is (571) 272-1665. The examiner can normally be reached on 8:30AM - 5:00PM Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tt  
December 6, 2004

  
**THIEN TRAN**  
**PRIMARY EXAMINER**